High-density **programmable** logic device in a multi-**chip** module package with improved interconnect scheme
RH Eng[3 ... - US Patent 5,642,262, 1997 - Google Patents
... and covers the sides as well as the top 100 and an FPIC 106 to create a fully ... Existing known-good-die maximizing the **probability** of finding near-neighbors. ... While the ment process uses the controlled-collapse **chip connection** above is a complete description of the preferred ...
Cited by 59 - Related articles - All 2 versions

A fault injection analysis of Virtex FPGA TMR **design** methodology [PDF] from ufrgs.br
F Lima, C Carmichael, J Fabula ... - Radiation and its ..., 2001 - ieeexplore.ieee.org
... case, if a single bit upset in the DUT routing matrix provokes an undesirable **connection** between two ... A bit flip in the customization logic will only be able to **generate** an mor if it ... exact same bit in two distinct redundant logic parts, which has an extremely low **probability** to occur. ...
Cited by 66 - Related articles - All 3 versions

Testing the 400 MHz IBM generation-4 CMOS **chip**
TG Foote, DE Hoffman, WV Huott ... - Test Conference, ..., 1997 - ieeexplore.ieee.org
... 8 storage controller/level2 (L2) cache chips, and a set of chips for clock distribution, cryptography and **connections** for the ... From this analyse, weights are assigned to each latch such that the **probability** of a 1 or 0 is assigned ... It then combines these patterns to create a weight set. ...
Cited by 20 - Related articles - BL Direct - All 4 versions

Test generation for current testing [CMOS ICs] [PDF] from upc.es
P Nigh ... - Design & Test of Computers, IEEE, 1996 - ieeexplore.ieee.org
... **probability** of a short between node Out and VDD is much lower than the **probability** of a ... a given input has only one VDD-to-GND path, we can detect the entire multiple-bridge **connection**. ... The methods for and details about the software that **generate** a list of possible IC faults are ...
Cited by 156 - Related articles - All 8 versions

An evolution programming approach on multiple behaviors for the **design** of application specific **programmable** processors [PDF] from psu.edu
W Zhao, ... - ... conference on Design and Test, 1996 - portal.acm.org
... PSA has three steps: 1 Sample the solution space in a **probabilistic** 6 2) u way(random y to get K ... An interest- ing thing is that the Crossover may **generate** the parent sometimes; this is not a problem because ... wr and wc are the weights for register and **connection** cost, respectively ...
Cited by 18 - Related articles - All 3 versions

High-performance cellular automata random number generators for embedded **probabilistic** computing systems
B Shackleford, M Tanaka, ... - ... 40th Conference on, 2002 - ieeexplore.ieee.org
... a neighborhood size of four and an asymmetrical, non-local neighborhood **connection** scheme. ... Recent improvements in reconfigurable technology now allow entire **probabilistic** computing systems to be ... on a single **chip** [1], [2]. However, the prob- lem of **generating** high-quality ...
Cited by 23 - Related articles - All 4 versions

[CITATION] Applications of combinatorics and graph theory to the biological and social sciences
FS Roberts - 1989 - Springer Verlag
Cited by 18 - Related articles - Library Search

TESTCHIP: A **chip** for weighted random pattern generation, evaluation, and **test** control
AP Stroele ... - Solid-State Circuits, IEEE Journal of ..., 1991 - ieeexplore.ieee.org
... and using (4) the **test** length necessary to get the same **probability** of detecting all the faults of F is ... There are sev- eral feedback **connections** between the tap positions. ... This requires much less hardware than **generating** parallel patterns simultaneously. ...
Cited by 55 - Related articles - All 4 versions

Method and apparatus for converting a **programmable** logic device designed into a selectable target gate array **design**
R I Kelley - US Patent 5,452,227, 1995 - Google Patents
... the general operation of the left path time increasing the reliability and **probability** of first ... time delay of the purpose computer 50 including an operator's console 52 input **connections** with respect ... and one represents the person of ordinary skill hi the art can create conversion flip ...
Cited by 72 - Related articles - All 2 versions

A generic architecture for on-**chip** packet-switched interconnections [PDF] from psu.edu
P Guerrier ... - ... conference on Design automation and test ..., 2000 - portal.acm.org
... We use a graph property of the fat-tree shown on figure 8: the graph is eulerian, thus a common prede- fined **connection** scheme can be applied to all routers to create paths covering all links and buffers in the network. ... 49% Load **Probability** of Occurrence ...
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